EFG Ribbon Technology R&D for Large Scale Photovoltaic Manufacturing

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ABSTRACT

We describe here the R&D programs carried out on Edge-defined Film-fed Growth (EFG) ribbon technology with DOE/NREL funding between 1998 and 2002 on the Phase 5A2 Manufacturing Technology Initiative, and the work and objectives for the 3-year continuation program in progress at this time.

1. Introduction

R&D on EFG technology at RWE Schott Solar Inc. (formerly ASE Americas) is focused on development of processes and equipment for large-scale manufacturing of silicon ribbon wafers, cells and modules. Industry-wide, construction of as many as 70 x 100 MW manufacturing facilities in the next two decades is required to address U.S. Photovoltaic (PV) Industry Roadmap targets [1]. Although crystalline silicon ribbon wafer production today constitutes less than 10% of the world PV total, it is one of the fastest growing segments of the PV industry. It is anticipated that EFG will maintain its position as a volume leader among ribbon technologies, as it makes use of the potential advantages of its technology in scaling up manufacturing [2]. In 2002, EFG technology capacities in Billerica were 21 MW for wafers and 5 and 8 MW for solar cells and modules, respectively. We are in the process of expanding cell and module capacity, first with a new 12 MW cell line in 2003, and we plan to increase cell and module manufacture to 20-25 MW beyond 2004 to match our existing EFG wafer capacity. We discuss here R&D on silicon ribbon wafer, cell and module technology ongoing in the program funded by NREL in support of these expansions in EFG manufacturing capacities, as well as plans for developing EFG technology for production of wafers up to 15 cm x 15 cm areas.

2. Ribbon Technology Cost Elements

The R&D carried out in our DOE/NREL programs have addressed cost elements of PV product manufacturing technology central to reducing costs in the most critical areas of product manufacturing. As shown in Figure 1, add-on costs for the individual areas of wafer, cell and module production processes are not evenly distributed, With other silicon manufacturing approaches, such as those based on wafer production by ingot casting or the CZ method, wafer production costs, in particular, dominate. Ingot and CZ wafer technologies cannot take advantage of the silicon material savings and reduced silicon contribution per wafer and per Watt in modules inherent to manufacture of modules based on ribbon wafers, where the ~50% kerf loss due to wafer cutting/sawing is avoided.

In our DOE/NREL programs we have, therefore, addressed all three areas of manufacturing, but with a specific concentrated emphasis on solar cell efficiency, which is a multiplier of costs in all three areas, and particularly on module cost reduction programs. In EFG ribbon wafer manufacture, emphasis has been on improving wafer electronic quality, on increasing yields, on raising productivity per crystal growth furnace, and on reducing labor costs in growth and laser cutting of wafers. Solar cell manufacturing cost reductions have been achieved through materials savings and process improvements which increase yields, decrease labor costs and increase throughput, and cell efficiency improvements. Module programs have had a special emphasis on a unique technology innovation in module design – the use of a reflecting material in the back plane of the module in order to reduce the effective number of cells required to achieve a given output power level. This "reflector module" has the potential to reduce the number of cells required by more than half, hence raising the effective solar cell efficiency to the order of 20%. In this paper, we highlight the past achievements in these areas, and outline the emphasis we will place on continuation programs in the new 3 year DOE/NREL program currently in progress.

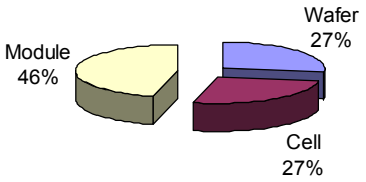


Figure 1. Cost breakdown among wafers cells and module add-on costs for typical ribbon module manufacturing.

3. Progress in PVMaT 5A2 from 1998 to 2002

New technology developments were undertaken in this time period concurrently with work to maintain manufacturing cost reductions with existing technology during expansion of our wafer manufacturing line from 4 to 20 MW. The higher capacity has leveraged these improvements and enhanced the competitiveness of EFG PV products. We worked on yield and throughput improvements through utilization of Statistical Process Control (SPC) methods, implemented supporting systems for computer aided databases and equipment and process tracking methodology for the purpose of handling large data fields, developed new diagnostic techniques, demonstrated a new dry etching process to reduce acid use and waste products, and formalized documentation and training procedures for manufacturing processes (ISO 9000) and for waste product and safety management (ISO 14000) to assist in handling the larger manufacturing organization. Low damage, high throughput laser technology was demonstrated, Rapid Thermal Processing approaches to improving cell efficiency were studied, and thin EFG wafer technology was evaluated using a cylinder tube configuration. EFG octagon and laser cutting technology larger than the standard 10 cm face tubes were developed to

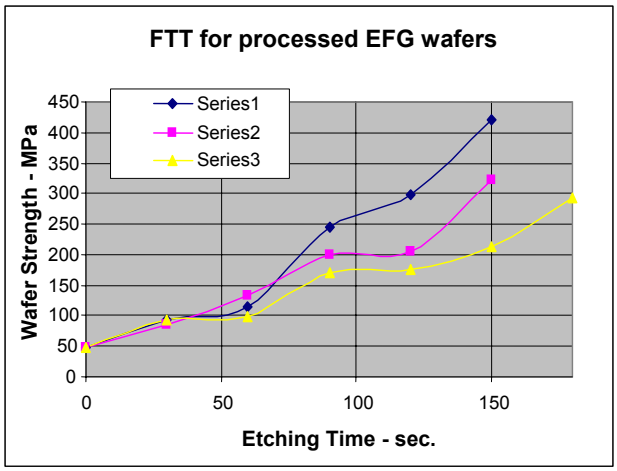
allow production of 12.5 cm x 12.5 cm wafers. In a task on Flexible Manufacturing methodology, we completed introduction of manufacturing databases for wafer and cell manufacturing, and process modifications to accommodate manufacture of 10 cm x 15 cm wafers, carried out module field performance studies and defect tracking to improve manufacturing processes, qualified and introduced into manufacturing a new encapsulant, and continued development of designs for low cost modules using a new reflector concept. We have reported on many of these details previously [3], and here will highlight those areas of previous activity from this earlier program that are continuing in the new 3-year program.

3.1 Wafer area production highlights. Ribbon module production technology at RWE Schott Solar is based on growth of polycrystalline silicon octagon-shaped thin-walled hollow tubes up to 6 m in length, and then cutting of the tubes into wafers using high speed lasers. Wafer cost reductions have been achieved in our program through reducing silicon feedstock consumption by silicon feedstock sorting and growth of thinner walled tubes; improving bulk wafer quality through advances in graphite purification techniques; increasing productivity per furnace with growth of larger diameter tubes, and widening the tube face; improving yields and reducing laser cutting labor costs through development of a new generation of high speed, low damage lasers; and introduction of larger wafer sizes by reconfiguring the laser cutter and etch processes to add the flexibility to switch between 10 cm x 15 cm wafers and standard 10 cm x 10 cm EFG wafers.

Since the wafer mechanical strength is a critical factor in determining yields all through the manufacturing line, a core element of our R&D programs in this area has been study of approaches to increase wafer strength both in the as-cut state, through laser beam quality improvements, and by optimizing post-cutting wafer etching. Unfortunately, a competing and compromising cost driver to improved cut quality is a higher cutting speed, which drives costs in cutting station throughput (capital costs) and labor utilization. Higher laser cutting speed typically requires higher power lasers that lead to poorer wafer cut edge quality. Since post-cutting etching costs decrease with a reduction in edge damage, these three elements all need to be taken into consideration and optimized in seeking out the lowest cost wafer production approach.

We have been successful in making improvements in all of these three areas of wafer production in the past PVMaT programs, and will continue to further develop lower cost laser cutting technology in our on-going program. A highlight of our progress in improving laser technology is illustrated through the data on fracture strength of EFG wafers shown in Fig. 2. We measure fracture strength through a specially designed fracture twist test (FTT), which we have developed to evaluate the specific limiting microcrack damage caused by laser cutting of silicon [4]. Both this type of plot, and the Weibull plots associated with it, establish the length of the residual microcrack in the as-cut it, establish the length of the residual microcrack in the as-cut state and after post-cutting processing, e.g., etching.

(a)



(b)

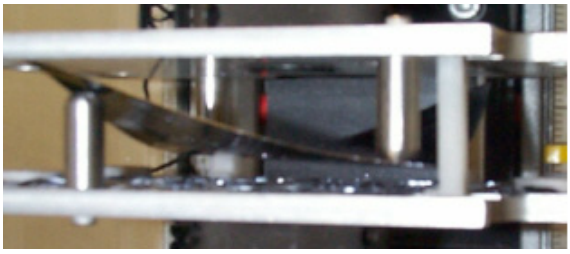


Figure 2. EFG wafer edge strength studies:
a) fracture twist test (FFT) results as a function of etch time;
b) side view of test apparatus with high strength EFG wafer shown edge on.

Each data point in Fig. 2a represents the average fracture strength in MPa for a lot of 20-25 EFG wafers. Each series represents a different post-cutting etching treatment. Etching strengthens EFG wafers to a remarkable degree. About one-third of the wafers in the batch of 25 representing Series 1 at the 150 s condition are deflected to the limits of the apparatus, (e.g., as shown in Fig. 2b), and do not break in this test, and so the averages in Fig. 2a underestimate their strength. It is anticipated that the intrinsic fracture strength of EFG silicon is controlled by defects in the as-grown wafer surface, and is in the range 1-1.5 GPa. Hence, the edge defects controlling fracture of wafers in the normal case are tending to get mostly eliminated in wafers such as shown in Fig. 2b.

Our work to date has identified several lasers which produce a reduced length of microcrack at cutting rates ranging from 50% to 300% greater than those being used in our manufacturing process currently. This allows optimization and cost reduction tradeoffs to proceed in two directions: either to minimize etching and waste product generation, or to maximize laser station throughput. An ongoing aspect of the work is to identify why some EFG wafers have fracture strengths below the statistical average strength, so that downstream yield losses can be reduced still more.

A second focus in EFG wafer development throughout the program has been on improving productivity per furnace. Tube diameter and face width are two important variants in

productivity. Pull speed is typically kept at the limit dictated by thermoelastic stress. Feasibility of growth up to a tube diameter of 50 cm was demonstrated for a cylindrical geometry [5]. On the basis of this work, smaller diameter prototype production units for growth of octagons with 12.5 cm face widths were designed and are now being evaluated for production of 12.5 cm x 12.5 cm EFG wafers. Barriers to expanding EFG tube diameters and face widths are the object of future R&D (see below). Industry trends have dictated the development of wafers with dimensions up to 15 cm x 15 cm, for which advantages are derived in downstream processing in cell and module fabrication. EFG tube technology has an added option - to cut and process different length segments from the tube cut along the growth direction, e.g., such as the 10 cm x 15 cm wafer production developed in this program, and with 12.5 and 15 cm widths.

Diagnostic method development was started in a number of areas, and is being continued to support process control and automation of wafer production. Feasibility studies were completed on sensors capable of measuring the deviations from flatness during crystal growth, and these will also be employed in automation of the crystal growth process. Evaluations of several techniques to detect cracks in wafers and cells were initiated. The most promising ones involve acoustic and laser (light) sensors, and this work is continuing in the ongoing program on developing robust equipment for in-line process monitoring. A program was started to examine the feasibility for measurement of residual stress using infrared (IR) polariscopy [6], and this method will be further evaluated in collaboration with several university teams in our next program.

3.2 Cell area improvement highlights. The PVMaT 5A2 program work scope included tasks on both cell efficiency improvements and development of new processes. Cell line process optimization was carried out with the help of SPC and Design of Experiments (DoE) in areas of junction properties, antireflection (AR) coating and metallization. A 40 finger front metal grid was introduced for use with thinner fingers. Efficiency gains were realized through bulk resistivity changes, increase of sheet rho in the diffused n-layer, and optimization of the AR coating. Production line averages were raised to the 14-14.5% range [7].

New process development proceeded with the exploration of Rapid Thermal Processing (RTP). Feasibility studies indicate that it is possible to obtain 15+% efficient cells with relatively short diffusion and metallization firing schedules [8]. At present, commercial equipment is not available which meets the throughput requirements and provide advances over current technology.

3.3 Module area improvement highlights. In this program, we completed tests on a new encapsulant, which has several advantages over our standard encapsulant. Among beneficial properties are that light transmission is improved by several percent, it has a lower level of moisture retention, and a higher melt flow index. This encapsulant also has superior adherence to glass. We evaluated the fire rating of our new encapsulant in a fire brand test and demonstrated that it passes the UL790 Fire Resistance Roof Covering Materials test, and achieves a class A fire rating.

We completed environmental testing of this new encapsulant and it has been introduced in manufacturing. The higher melt flow index allows lower lamination temperatures to be used, and this has increased throughput and decreased labor costs. Increased yields also have been achieved because less pressure is exerted on cells during lamination. Its good UV cutoff and increased transmission in other parts of the spectrum contributes to a gain of 2-3% in module performance. Our standard encapsulant is sensitive to moisture. If flux solute is not completely evaporated during the interconnect process, or trapped in the solder joint, then the water content eventually leads to a discoloration in the solder joint area. This cosmetic problem is now eliminated.

The affinity of our standard encapsulant for water further has required the use of a moisture barrier in the back of the module to prevent water from entering, *viz.*, our standard double glass (DG) module construction, or a vapor barrier in the backskin. The availability of this new encapsulant, without the necessity that it be sealed against moisture ingress, now allows us to proceed to a new module platform. This platform will preserve the most desirable features of our double glass module, while reducing module weight and cost.

Prototype development of the reflector module, which we first evaluated in our PVMaT 4A2 program [9], is ongoing. This work has been interrupted and delayed several times due to inability to obtain a consistent quality of material with a process which has potential for scaling up to large manufacturing levels.

4. New manufacturing technology R&D program

Demands for improved manufacturing processes and reduced costs for EFG ribbon-based products have served to refocus the new development program. Work has been accelerated in several areas critical to proving technology which have significant module cost reduction potential: 1) large diameter EFG tubes and wider faces; 2) laser evaluation and wafer strength optimization; 3) data acquisition and management for high capacity manufacturing; 4) in-line diagnostics and growth process automation; 5) and reflector module development. Progress in these areas is described next.

4.1 Large diameter EFG Systems and wafers. In the first year of this program, we have emphasized further development of hot zones with improved growth stability and reduced stress for large diameter octagon growth and increased wafer dimensions. Barriers are being addressed with thermal modeling [10] in design of hot zones. Long lead times are required for procurement of components, while to obtain detailed information on post-growth cooling profiles along the ribbon growth axis requires time consuming experiments using thermocouples and are difficult to interpret. The models provide detailed information in both of these areas and information turn-around is greatly enhanced in efforts to reproduce known stable growth and low stress temperature profiles.

Development is currently underway for optimizing growth and reducing stress effects in a 12.5 cm face

octagon. Since thermoelastic stress effects increase in severity with increasing face width, the current strategy is to apply methods for stress reduction to this intermediate dimension of wafer, and find stress reduction configurations in working to the 3 year program goal of demonstrating growth systems with 15 cm octagon faces.

4.2 Laser cutting and wafer strength optimization. Study of factors affecting laser cutting quality is ongoing in order to find an optimum combination of cut speed, edge damage reduction and post-cutting etching treatments that maximize wafer strength. We have installed one new laser and are undergoing production line trials and wafer strength studies. This laser can cut up to speeds 60% greater than what we have on the production line at this time, and this is coupled with a reduction in microcrack length by ~50%. We are in the process of evaluating a second laser with comparable quality which has potential to cut at speeds 300% above our baseline. The performance of these lasers will be evaluated and advantages in wafer quality determined in the coming year.

4.3 High capacity manufacturing database development. Data acquisition and database management for rapid turnaround of information contributes to diagnostic capabilities and are crucial to optimization of line performance and in diagnosing faulty equipment or process performance. We are proceeding in a task to extend the previous systems developed in the wafer production area to cell and module manufacture. As we deploy our new 12 MW cell line this year, the work scope in this task will be to extend and integrate the data systems and equipment monitoring and diagnostics to both cell and module areas. To date, we have installed and are integrating new data tracking systems for Total Preventative Maintenance (TPM) implementation.

4.4. In-line diagnostics. We have completed surveys of diagnostic equipment suitable for in-line monitoring of various critical machine and process variables, and will plan to continue with feasibility demonstrations over the course of our new 3 year program. The areas that will be investigated include crystal growth temperature control, EFG tube thickness and flatness, wafer and cell cracks, interconnect bonds, wafer bulk electronic quality and module materials.

4.5 Reflector Module. Several new vendors for reflector material have been evaluated in the past year, and experimental modules made to measure performance characteristics and reliability with various materials and encapsulants. Table 1 indicates the performance enhancement that we have demonstrated in a number of promising embodiments. The current and voltage enhancements all are calibrated against a reference cell tested under identical outdoor illumination under a clear sky with the same insolation and temperature conditions. A 60% enhancement factor demonstrates a potential to reduce module costs (see Fig. 1 for reference) by being able to produce the same power from a given module area after taking out 40% of the cells.

Table 1. Percent delta enhancements in open circuit voltage Voc (V) and short circuit current Jsc (mA/cm^2) for various reflector configurations, with best case highlighted.

Case	W/O Reflector		With Reflector		Percent Delta	
	Voc	Jsc	Voc	Jsc	Jsc	Voc*Jsc
1	1.00	30.3	1.02	47.4	56	60
2	1.74	29.2	1.79	43.8	49	54
3	1.77	32.0	1.81	45.6	43	46
4	**1.80**	**29.9**	**1.84**	**50.0**	**67**	**71**
5	1.84	30.8	1.86	48.4	57	59

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